REMARKS

Claims 1-20, 22-27, and 37-39 are pending in the application, of which Claims 1, 6, and 12 are independent claims. Claims 9, 11, 17, 19, and 20 are withdrawn from consideration, and Claims 1-8, 10, 12-16, 18, 22-27, and 37-39 are rejected under 35 U.S.C. § 103(a).

Claims 1-4, and 37 are rejected under 35 U.S.C. § 103(a) based on Wilska (UK 2,289,555) in view of Takahara et al. (US 5,436,535) and Helms (U.S. 5,760,760). Claim 5 is rejected under Section 103(a) based on Wilska in view of Takahara, Helms, and further in view of Shigeta et al. (US 5,394,204). Claims 6-8, 10, 12-16, 18, 22-27, 38, and 39 are rejected under Section 103(a) based on Wilska, in view of Takahara, Helms, Shigeta, and Yagyu (US 5,856,814). Reconsideration is respectfully requested.

At issue remain the teachings of Takahara and Helms. As now claimed, the Applicants employ a power management circuit to lower the power consumption of a display control circuit. As claimed, image data received by a receiver is input to the display control circuit which generates a display signal including a vertical synchronization signal to drive the matrix display to render the image. A light emitting diode source illuminates the display. The power management circuit lowers the power consumption of the display control circuit between vertical synchronization signals.

As further expressly recited, the power management circuit is arranged to receive control signals for lowering the power consumption, whereby the control signals result from signals from the display control circuit that are initiated by the display control circuit. The power management circuit and the display control circuit are connected together and arranged in a configuration that lowers the power consumption in a self regulating manner.

For example, referring to FIG. 2C, circuit 122 can transmit control signals to backlight 111 and display 112 along lines 115-118. The power management circuit 123 can receive control signals along line 126 from circuit 122 to lower power consumption of the circuit 120. The power management circuit 123 can be connected by line 129 to flash memory circuit 125, the digital-to-analog converter, the buffer/inverter, and display 112, and can control power during display operation, including, for example flash illumination by the backlight during color sequential or monochrome operation. The use of a thin film active matrix circuit can store charge between vertical synchronization pulses which can enable lower power consumption.

The control signals from circuit 122 to the power management circuit 123 are initiated by the circuit 122 so that the power consumption can be considered lowered in a self-regulating manner.

In contrast, in FIG. 22 of Takahara, battery 222 provides power to light emitting tube power supply circuit 223, display device drive circuit 224 and the reproduction circuit 225. Electrical power to light emitting tube 211 is provided by light emitting tube power supply circuit 223. Video signals are provided to display device 214 from display device drive circuit 224, which in turn receives signals from either CCD sensor 221 or reproduction circuit 225.

Takahara teaches modulation of the anode voltage to light emitting tube 211 with a pulse signal, which cycles at 60 Hz to lower the power consumption of light emitting tube 211, and where the pulse width is varied by manually rotating a variable resistor on the camera (Col. 31, lines 38-40). By varying the pulse width, the quantity of emitted light can be varied proportionately. Using a 50% pulse width, the power consumption of the light emitting tube is said to be reduced to 0.25 W. Adding in the power consumption of the LCD brings the power to "slightly greater than 0.3 W" (Col. 31, l. 62). Consequently, the power consumption is lowered only when the pulse width is varied by manual user-initiated external input and is merely a power level setting. There is no lowering of power consumption after the power level setting is made. As a result, there is no structure, capability or suggestion of lowering power consumption in a self regulating manner.

Helms discloses in FIG. 2, a system block diagram of PC 10, having a CPU 200, system RAM, I/O devices 206, and brightness control circuitry 204 having a processor 204a, memory 204b and an analog/digital converter 204c for controlling the brightness level of LCD panel 12. Control knob 16 and photodetector 14 are connected to the brightness control circuitry 204. The brightness of LCD panel 12 can be manually raised or lowered by control knob 16. Using manual knob 16 does not lower power consumption in a self regulating manner. In addition, the brightness can be maintained, or raised or lowered to a viewable level by photodetector 14, based upon the surrounding ambient light.

Photodetector 14 senses the amount of ambient light, and then provides ambient light signals AL corresponding to the amount of sensed light to processor 204a of brightness control circuitry 204 via line 212. A plurality of automatic brightness level signal values ABL are stored

in memory 204b of brightness control circuitry 204 corresponding to possible ambient light signal valves AL, and can be in a look-up table. Processor 204a of brightness control circuitry 204 is provided with corresponding automatic brightness level signal ABL from memory 204b. If processor 204a determines there is a new ambient light signal AL, processor 204a outputs the appropriate brightness control signal BC on line 210 to LCD Panel 12 for increasing or decreasing brightness. When the brightness is increased, power consumption is increased. If processor 204a determines there is no change in the ambient light signal AL, no brightness control signal BC needs to be sent by processor 204a. The look-up entries for AL signals can be altered by user adjustments with control knob 16 which generates signals USBL. Signals AL, ABL and USBL are merely logic signals that are considered by processor 204a of the brightness control circuitry 204. The actual control signals are brightness control signals BC that are sometimes generated by processor 204a of the brightness control circuitry 204, and sent to LCD 12 depending upon the analysis of signals AL, ABL and USBL. As a result, brightness control circuitry 204 receives and analyzes logic signals and generates control signals. Brightness control circuitry 204 and processor 204a do not receive control signals for lowering the power consumption as specified in the claimed invention, and often increases power consumption.

Accordingly, Claims 1-8, 10, 12-16, 18, 22-27, and 37-39, as amended, are not obvious in view of Wilska, Takahara and Helms, together, or further in view of Shigeta and Yagyu, since none of the references, alone or in combination, teach or suggest a "power management circuit arranged for receiving control signals for lowering the power consumption, the control signals resulting from signals from the display control circuit that are initiated by the display control circuit, the power management circuit and the display control circuit being connected together and arranged in a configuration that lowers the power consumption in a self regulating manner", as recited in base Claims 1, 6 and 12. Therefore, Claims 1-8, 10, 12-16, 18, 22-27, and 37-39, as well as Claims 9, 11, 17, 19, and 20, are now in condition for allowance. Reconsideration is respectfully requested.

CONCLUSION

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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